MAR 0 1 2004

CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this correspondence (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Nonmissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February , 2004.

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Laura Lee Mosier

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Yoshihide SENZAKI

Serial No. 10/

10/766,148

January 27, 2004

For: Multilayer High K Dielectric Films

And Method of Making Same

Art Unit:

To be assigned

Examiner:

To be assigned

Date:

February 25, 2004

INFORMATION DISCLOSURE STATEMENT SUBMITTED PRIOR TO THE FIRST OFFICIAL ACTION

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Filed:

Applicant submits herewith patents and publications which may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. §1.56. While this Statement may be "material" pursuant to 37 C.F.R. §1.56, it is not intended to constitute an admission that any patent, publication, or other information referred to therein is "prior art" for this invention unless specifically designated as such.

Enclosed herewith are PTO/SB/8A and PTO/SB/8B forms listing art potentially relevant or of interest to the referenced patent application. This application relies on the earlier filing date of prior Application No. 10/056,625, filed January 25, 2002, under 35 U.S.C. § 120. It is understood that the Examiner will consider information that was submitted to or cited by the Office in such prior applications. Copies of documents previously submitted to or cited by the Office in the prior application are not required to be provided in this application and thus are not attached. 37 C.F.R. § 1.98(d).

To satisfy the duty of disclosure under 37 CFR § 1.56 and MPEP § 2001.06(b), Applicant notes that the present application is related to pending U.S. Application Serial No. 10/056,625, filed January 25, 2002 and U.S. Application No. 10/766,618 filed January 27, 2004.

This information disclosure statement is being filed in compliance with 37 CFR § 1.97(b)(3) as being filed before the mailing date of the first office action on the merits.

Should any questions or comments arise regarding the listing of the submitted publications and patents in which the Examiner feels a telephone conversation would be appropriate, he or she is respectfully requested to contact the undersigned attorney at the listed telephone number.

Respectfully submitted,

DORSEY & WHITNEY LLP

Tianjun Hou

Reg. No. 51,821

Suite 3400, Four Embarcadero Center

San Francisco, CA 94111-4187

Telephone: (650) 494-8700 Facsimile: (650) 494-8771

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PTO/SB/8A (08-00)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)						Application Number Filing Date		10/766,148				
									January 27, 2004 Yoshihide SENZAKI			
							First Named Inventor					
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^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.

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PTO/SB/8B (08-00)

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INFORMATION DISCLOSURE					Application Number	10/766,148				
				PPLICANT	Filing Date	January 27, 2004				
				_	First Named Inventor	Yoshihide SENZAKI				
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	C1	MANCHANDA et al., "Si-Doped Aluminates for High Temperature Metal-Gate CMOS: Zr-Al-Si-O, A Novel Gate Dielectric for Low Power Applications, 2000 <i>IEEE</i> , pp. 15-18.								
	C2	WILK et al., "Electrical Properties of Hafnium Silicate Gate Dielectrics Deposited Directly on Silicon", Applied Physics Letter, vol. 74, 1999, pp. 2854-2856.								
	C3	WILK et al., "Stable Zirconium Silicate Gate Dielectrics Deposited Directly on Silicon", Applied Physics Letters, vol. 76, no. 1, January 3, 2000, pp. 112-114.								
	C4	WOLFE, D., et al., "Remote Plasma Enhanced-Metal Organic Chemical Vapor Deposition of Zirconium Oxide/ Silicon Oxide Alloy, $(ZrO_2)_x$ - $(SiO_2)1_x(x \le 0.5)$, Thin Films for Advanced High-K Gate Dielectrics", <i>Materials Research Society Symposium</i> , vol, 567, 1999, pp. 343-348.								
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